# VARIABLE GATE BIAS FOR A REFERENCE TRANSISTOR IN A NON-VOLATILE MEMORY

## ABSTRACT

A non-volatile memory (30) comprises nanocrystal memory cells (50, 51, 53). The program and erase threshold voltage of the memory cell transistors (50, 51, 53) increase as a function of the number of program/erase operations. During a read operation, a reference transistor (46) provides a reference current for comparing with a cell current. The reference transistor (46) is made from a process similar to that used to make the memory cell transistors (50, 51, 53), except that the reference transistor (46) does not include nanocrystals. By using a similar process to make both the reference transistor (46) and the memory cell transistors (50, 51, 53), a threshold voltage of the reference transistor (46) will track the threshold voltage shift of the memory cell transistor (50, 51, 53). A read control circuit (42) is provided to bias the gate of the reference transistor (46). The read control circuit (42) senses a drain current of the reference transistor (46) and adjusts the gate bias voltage to maintain the reference current at a substantially constant value relative to the cell current.